Subt D2

24. (Amended) The microelectronic device of claim 22 [23], further comprising a silicide layer formed on [over] the [polysilicon] adhesion layer.

25. (Amended) The microelectronic device of claim 22 [23], further comprising a conductive [tungsten silicide] layer formed on [over] the [polysilicon] adhesion layer.

Subt D3

26. (Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide extending from the trench[,] beyond the surface of the substrate; and

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

Subt D3

28. (Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide extending from the trench[,] beyond the surface of the substrate; and

C3

a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

Subt D4

30. (Amended) A microelectronic device, comprising:

a microelectronic substrate having a recess formed in a surface thereof; and

C4

a field oxide deposited in the recess [trench], the field oxide extending from the recess [trench] beyond the surface of the substrate[,] by a height which is less than or equal to approximately one half of a height of a component formed on the field oxide.

Subt D5

32. (Twice Amended) A microelectronic device, comprising:

C5

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate, the gate structure including a gate oxide layer formed on the microelectronic substrate, a first gate layer formed on the gate oxide layer, an adhesion layer composed of a material other than a conductively doped polysilicon material formed on the first gate layer, and a conductive layer formed on the adhesion layer; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate.

34. (Amended) A microelectronic device, comprising:

a microelectronic substrate having a trench formed therein;[,]

a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide [pad]; and

a component formed on the field oxide.

REMARKS

Claims 22 and 24-37 are pending in the present application. In the Office Action dated August 2, 2000, the Examiner (1) rejected claims 30-31 under 35 USC §112, second paragraph, as being indefinite; (2) rejected claims 22, 32, and 34-36 under 35 USC § 102(b) as being anticipated by Manning (US 5,177,028); and (3) rejected claims 22-37 under 35 USC § 102(e) as being anticipated by Matsumoto *et al* (US 5,726,479).

Applicants respectfully request reconsideration of claims 22 and 24-37 in view of the foregoing amendments and the following remarks. Some of the technical differences between the applied references and embodiments of the invention will now be discussed. Of course, these discussed differences regarding the embodiments, which are disclosed in detail in the patent specification, do not define the scope or interpretation of any of the claims. Where presented below, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Generally, the disclosed embodiments are directed to methods and apparatus having trench isolation structures with reduced isolation pad heights and reduced edge spacers. In one embodiment, an apparatus comprises a semiconductor substrate, a gate oxide layer formed on the substrate, and a first gate layer formed on the gate oxide layer. A trench